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Short channel effects and drain field relief architectures in polysilicon TFTs

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Applications of polycrystalline silicon (polysilicon) thin film transistors (TFTs) to active matrix organic light emitting displays require further performance improvement. The biggest leverage in circuit performance can be obtained by reducing channel length from the typical current values of 3-6μm to 1μm, or less. However, short channel effects and hot-carrier induced instability in scaled down conventional self-aligned polysilicon TFTs can substantially degrade the device characteristics. To reduce these effects and allow proper operation of the circuits, drain field relief architectures have to be introduced. In this work we show that a fully self-aligned gate overlapped lightly doped drain (LDD) structure, with submicron LDD regions, can provide an excellent solution, allowing effective short channel effect control and improved electrical stability.

Introduction

Low temperature polycrystalline silicon (polysilicon) thin film transistor (TFT) technology is of great interest for active matrix organic light emitting displays (AMOLED), particularly for the latest generation of high resolution mobile phone displays [1]. The non-uniformity in the electrical characteristics of polysilicon TFTs, which is a major limitation for producing high-image-quality AMOLEDs [2], has been recently tackled by introducing increased complexity into the pixel circuits, by compensating for both threshold voltage and field effect mobility variations [3-5]. However, some compensating circuits, such as current programming methods, require very high addressing speeds for high resolution displays [4]. In addition, electrical stability is a critical requisite of the driving TFT in AMOLED applications. In order to improve circuit performance, needed for both compensating pixel circuits as well as for integrated drivers, reduction of channel length, from the typical current values of 3 μm to 1 μm or less, is being pursued. As a result, short channel effects [6] and hot carrier induced instability [7] in scaled down self-aligned (SA) polysilicon TFTs become a serious issue, and drain field engineering is mandatory. In this work we review the effects of downscaling the device geometry and, in particular, the kink effect, threshold voltage variations and hot-carrier induced instability are examined in some detail by combining experimental measurements and two-dimensional numerical simulations. In order to mitigate short channel effects and improve electrical stability, the introduction of drain field relief architectures is essential, and the advantages and disadvantages of the most popular architectures adopted to improve the device performance, including lightly doped drain (LDD) and gate overlapped LDD (GOLDD) structures, are discussed. Finally, the

experimental data of the fully self-aligned GOLDD (FSA-GOLDD) polysilicon TFTs, with submicron LDD regions, are presented. We show that such advanced device architecture can provide substantial reduction of short channel effects and improve hot-carrier induced instability.

Device fabrication

Conventional self-aligned (SA) short n-channel (down to 0.4 μm) TFTs used in this work were fabricated according to a process reported in Ref. [8]. The polysilicon active layer, 40 nm thick, was crystallized by excimer laser annealing. Source and drain contacts were formed by implanting P-ions to a dose 10^{15} cm^{-2} through the oxide film, with the gate acting as a mask, and doping activation was obtained by a second pass through excimer laser. The gate oxide was deposited in a PECVD system, using SiH_4 and N_2O gas mixture, and, unless specified, the thickness was 62 nm. FSA-GOLDD polysilicon TFTs were fabricated according to the process flow reported in Ref. [9]. The initial key stage in forming FSA-GOLDD TFTs is the sputter deposition of a 1μm thick film of Al(1%Ti) as the gate metal, and its reactive ion etching to leave near-vertical side wall angles, greater than 85° for the gate pattern. The first self-aligned step is then to implant an LDD region (4 different ion doses have been adopted: $6x10^{12}$, $9x10^{12}$, $1.5x10^{13}$ and $2.5x10^{13}$ cm^{-2}) using the gate metal as the implant mask. Following this, the second key stage is to form the sidewall spacers by conformally depositing the conducting 0.5 μm thick PECVD n^+ amorphous silicon (a-Si) layer. Anisotropic reactive ion etching of the conformal n^+ a-Si layer yields the sidewall spacer features attached to the vertical sidewalls of the gate metal. The second self-aligned step uses the gate metal plus sidewall spacers as a mask for the high dose ion implantation to form source and drain contacts self-aligned to the LDD regions. One general rule of thumb from the MOSFET industry is that the width of the sidewall spacer is about 2/3rds the height of the vertical sidewall (provided the thickness of the spacer material is ≥ the gate height). Thus, with 0.5 μm thick gate metal, we can expect sub-micron self-aligned field relief regions of the order of 0.35 μm.

Short channel effects in polysilicon TFTs

Short channel effects have been well established, and widely studied, in c-Si MOSFETs [10], and they refer to a range of phenomena for which the classical long channel model no longer applies. When reducing device channel length, L, short channel effects are displayed as threshold voltage decrease with decreasing L (V_T roll-off) and with increasing source-drain voltage (V_{ds}), subthreshold slope variations and poor saturation in the output characteristics. These are a consequence of a number of inter-related phenomena, such as the size of the source and drain space charge regions becoming comparable to channel length, which reduces the amount of charge needed on the gate to invert the channel surface, and this reduces the threshold voltage with reducing channel length. Also, when the drain space charge region is comparable to channel length, such that the source and drain space charge regions start to overlap, increased drain bias can reduce the potential barrier between the source and the channel (drain-induced barrier lowering, DIBL), giving drain-bias-dependent sub-threshold currents and poor current saturation in the output characteristic. In addition, since polysilicon TFTs are fabricated on insulating substrates, floating body effects take also place [11] and are enhanced by L-

reduction. In the followings, we will describe in some detail short channel effects observed in conventional self-aligned polysilicon TFTs.

Kink effect

In general, the output characteristics of polysilicon TFTs show, at high V_{ds}, an anomalous current increase, often called "kink" effect [11] in analogy with SOI devices [12]. Two-dimensional numerical simulations have shown that the kink effect is caused by impact ionization at the drain end of the channel, due to the large drain field when the device is operating in saturation. In addition, the kink effect is also enhanced by a parasitic bipolar transistor (PBT) action [13], similarly to floating body effects observed in SOI-devices. Impact ionization generated holes are injected into the floating body (base) forcing further electron injection from the source (emitter), which are then collected by the drain (collector). This added drain current augments the impact ionization, which in turn drives the floating body harder, thereby causing a regenerative action leading to a premature breakdown. Output characteristics have been measured for different L and compared at relatively low V_g (just below the threshold voltage, i.e. around 2.1 V), so that the characteristics were not affected by the parasitic resistance effect.
In Fig. 1a, typical I_d-V_{ds} characteristics are shown for different L, measured for V_g around V_T and adjusted to maintain the same low-field normalised output conductance, g_{d0}xL. As can be seen, both saturation current and kink effect appear very sensitive to channel length reduction. In particular, for short channel devices, the characteristics no longer saturate and kink effect becomes very serious. Channel length reduction also results in an increase in the output conductance, g_d, and the minimum normalised output conductance value, g_{dmin}/g_{d0}, shows an L^{-1} dependence (see Fig. 2). Output conductance increase has an adverse effect in circuit applications, as it increases in digital circuits the power dissipation and slightly degrades the switching characteristics, while, in analogue circuits, it reduces the maximum attainable gain as well as the common mode rejection ratio.
The kink effect was analyzed by using two-dimensional numerical simulations and by adopting the effective medium approximation. By using a single set of optimized parameters for the density of states (DOS) and impact ionization parameters [14], it was possible to accurately reproduce the kink effect variation with L, as can be realized by comparing experimental (Fig. 1a) and simulated (Fig. 1b) output characteristics. From the simulated output characteristics we deduced the g_{dmin}/g_{d0}, also reported in Fig. 2, and we found a very good agreement with the trend shown by the experimental data. To confirm the role of the kink effect on the drain current increase, we simulated the output characteristics by turning off the impact ionization and the corresponding curves are reported in Fig. 1b. It can be seen, by comparing the output characteristics with and without impact ionization, that the drain current at high V_{ds} is dominated by the kink effect, while DIBL has only a limited effect on the saturation drain current increase.

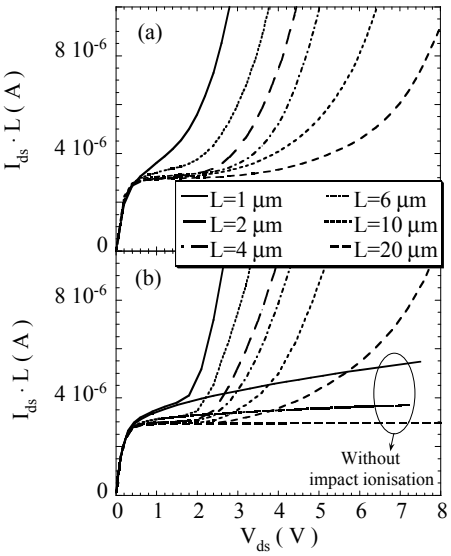

Figure 1. Experimental (a) and simulated (b) output characteristics for Vg=2.1 V (just below threshold voltage) and different channel length, L. Simulated characteristics have been calculated by including impact ionization mechanism, and for L=1, 2 and 6 µm we also show the characteristics obtained by turning off the impact ionization.

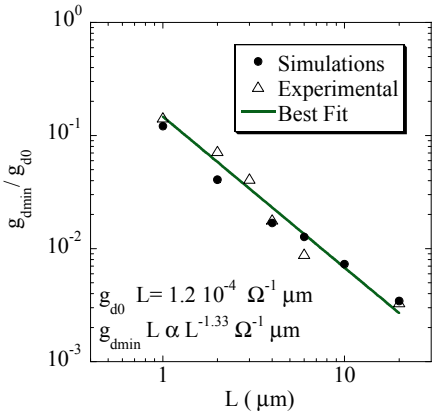

Figure 2. Experimental and simulated g_{dmin}/ g_{d0} vs channel length, L.

Threshold voltage and subthreshold slope

Threshold voltage is known to be reduced in short channel MOSFETs by decreasing channel length and increasing source-drain voltage. This effect was explained by Troutman [15] by analyzing the electrostatics of short channel MOSFETs: as the channel length is reduced, source and drain electric fields penetrate deeply into the middle of the channel, lowering the potential barrier between source and drain and determining a lower V_T with respect to the long channel case. Moreover, when a high drain voltage is applied to a short-channel device, the barrier height is lowered even more, resulting in a further V_T decrease (drain induced barrier lowering – DIBL [15]). However, in polysilicon TFTs, commonly fabricated on insulating substrates, floating body effects also represent another important factor influencing V_T. Indeed, as discussed in the previous section, the presence of high electric fields at the drain end of the channel triggers impact ionization and excess

carriers are injected into the floating body giving rise to PBT effect. Therefore, in short channel polysilicon TFTs threshold voltage variations are, in general, due to a combination of mechanisms, including floating body effects, drain induced barrier lowering and field enhanced mechanisms.

In fig. 3, typical $I_d - V_g$ characteristics, measured on devices with channel widths (W) equal to 50 µm and two channel lengths at different drain bias, V_{ds}, are shown. The transfer characteristics of the shortest L show an appreciable shift of the threshold voltage, a degradation of the subthreshold slope and an increased spread in the transfer characteristics as V_{ds} increases, denoting a substantial threshold voltage variation with V_{ds}. In order to quantify the variation of threshold voltage as a function of L and V_{ds} , we defined V_T as the gate voltage at which $I_d = 10^{-7}$ A × W/L. In Fig. 4 the V_T dependence upon V_{ds} is shown for devices with channel length ranging from L=0.4 µm to L=20 µm. As can be seen, while in the long channel devices no V_T dependence upon V_{ds} is observed in the moderate and high drain bias region of the plot, in the short channel devices V_T is decreased for increasing V_{ds} , which is similar to that observed in c-Si MOSFETs. Fig. 5 shows the dependence of V_T upon the channel length for three different drain bias: it is clear that as V_{ds} is increased the V_T curves tend to spread out, denoting an increased V_T roll-off with L. This is a finding in contrast with what is observed in SOI devices, where increasing V_{ds} reduces the V_T roll-off as channel length is reduced [16].

To clarify the short channel effects we used numerical simulations, adopting as already mentioned, the effective medium approximation [11, 14]. The device characteristics were reproduced very accurately, using the set of optimized parameters reported in ref. [17] and the threshold voltage was then evaluated from simulated transfer characteristics, using the same criterion adopted for the experimental data.

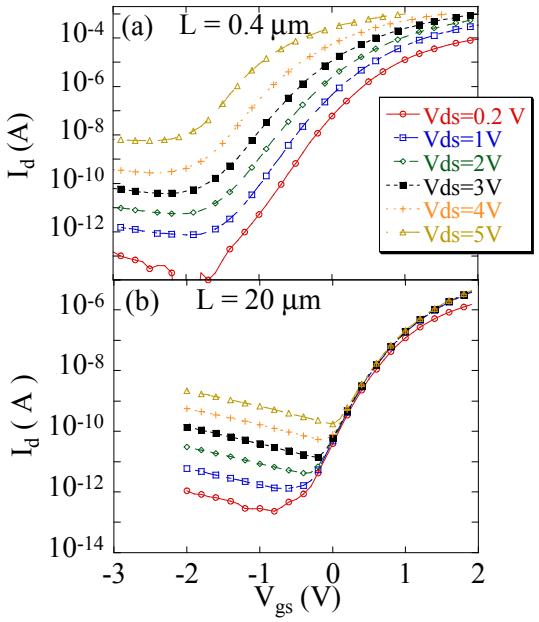

Figure 3. Experimental transfer characteristics, for a device with L = 0.4 µm (a) and L = 20 µm (b), measured at different V_{ds}.

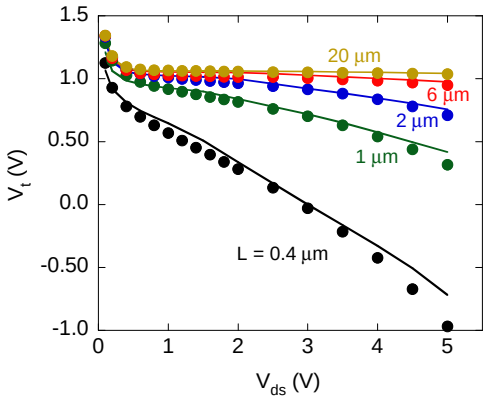

Figure 4. Experimental (symbols) and simulated (continuous lines) V_T as a function of drain bias for devices with different L. Simulations include the impact ionization model.

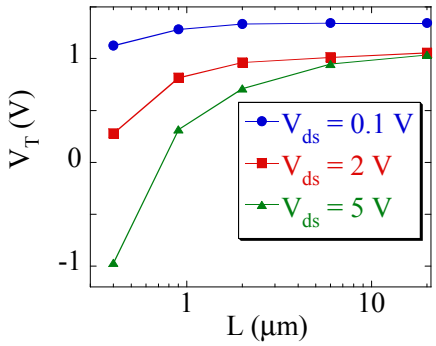

Figure 5. Threshold voltage, V_T, as a function of channel length L measured at three different drain bias.

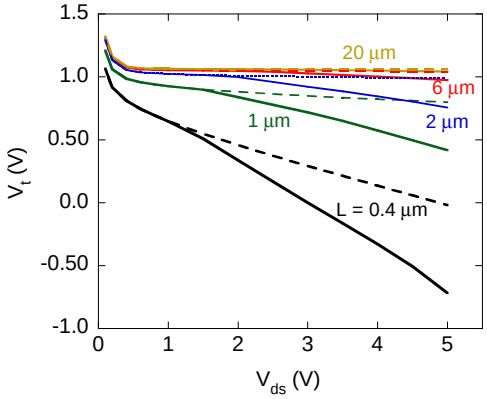

Figure 6. Simulated V_T for devices with different channel length. Simulations are performed with (continuous lines) and without (dashed lines) the impact ionization model.

The simulated V_T data nicely reproduce the dependence upon V_{ds} observed experimentally (see Fig. 4). Given the presence of impact ionization in the simulated results, the relative contributions of the direct DIBL and the PBT effects, which will also lower the source-channel barrier, can be also evaluated [17]. Figure 6 shows the

simulations of V_T, with and without the impact ionization turned on, demonstrating that at low V_{ds} the DIBL was primarily responsible for the barrier lowering, but the effect of hole accumulation, via the PBT effect, reduced the barrier at higher values of V_{ds}. As would be expected from Fig. 3, both effects increased as the channel length decreased.

Hot-carrier induced instability

The presence of high electric fields at the drain junction combined with the high electron mobility leads to carrier heating. Hot-carriers can generate defects at the Si/SiO_2 interface and charge trapping in the gate oxide, inducing degradation of the device characteristics [18]. Extensive investigation of hot-carrier effects in polysilicon TFTs has shown that, similarly to c-Si MOSFETs, the device degradation is controlled by the formation of interface states and injection of charge in the gate oxide [19, 20]. By using numerical simulations, based on the interface state formation mechanism related to the sequential trapping of holes followed by electron capture (two-step model [21]), it has been demonstrated that hot-carrier induced damage is localized at the drain end of the channel at both front and back interfaces and a precise evolution of the damaged region during bias stress has been provided [19, 20].

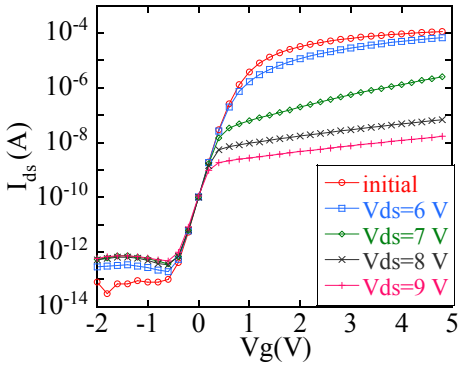

Figure 7. Transfer characteristics measured at V_{ds}=0.1 V during an accelerated stability test (see text) for SA polysilicon TFT with L=1.5 μm.

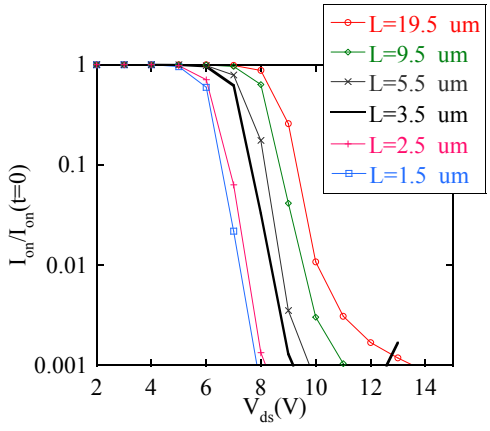

Figure 8. Relative on-current variation, measured at V_g=5 V and V_{ds}=0.1 V, during accelerated stability tests (see text) performed is SA polysilicon TFTs with different L.

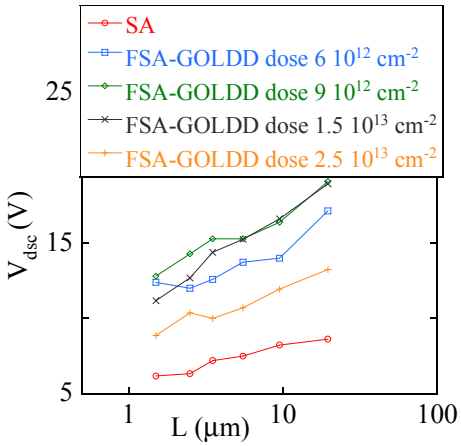

Figure 9. Critical drain bias, V_{dsc}, needed in accelerated stability test to produce 50% on-current reduction for SA and FSA-GOLDD devices with different LDD doses (as indicated) vs device channel length L.

In Fig. 7 the effects of an accelerated stability test in a SA TFT are reported: bias stress was performed for 60 seconds at $V_g=V_T$ with a given V_{ds} and the transfer characteristics were re-measured after bias stress, then the bias stress V_{ds} was incremented and the cycle repeated. As can be seen, increasing V_{ds} produces a marked degradation in the device characteristics and stronger degradation appears in short channel TFTs. In Fig. 8 the relative on-current variation vs bias stressing V_{ds} is reported for different L, showing that device degradation occurs at lower V_{ds} as L is decreased. This is more clearly evidenced in Fig. 9, where the bias-stressing V_{ds} needed to reduce to 50% of the initial on-current value (V_{dsc}) is reported for different L. From these data we can conclude that reducing L has an adverse effect on the hot-carrier induced instability, since reducing L implies higher electric fields at the drain junction, for a given V_{ds}, and, consequently, more carrier heating.

Drain field relief architectures

As shown in the previous section, short channel SA polysilicon TFTs suffer substantial electrical characteristic degradation, and drain field engineering is mandatory in view of device downscaling. Indeed, the LDD architecture has been shown to improve short channel effects [22] and electrical stability [20], although at the expenses of increased parasitic resistance [20]. Series resistance can be substantially reduced in the GOLDD structure [23], where the gate-drain overlap capacitance can be minimized by adopting a fully SA process using conductive sidewall spacers [9, 24, 25]. GOLDD structures have been demonstrated to provide excellent drain field relief with reduced series resistance [23], however, the benefits of reducing channel length could be cancelled out by series resistance and overlap capacitance from disproportionately large field relief regions. Definition of submicron LDD regions is therefore essential, and several processes have been proposed [9, 24, 25]. Originally, Hatano et al. [24] fabricated FSA-GOLDD devices by using doped polysilicon sidewall (defining LDD regions 180 nm in length) and showed the superior performance of FSA-GOLDD devices with respect to LDD or SA TFTs. The process was inspired by the well-known technology of single crystal silicon MOSFETs, namely, the use of sidewall spacers acting as sub-micron and self-aligned masks for implant and etch processes. Mishima et al. [25] also proposed a simplified

method for forming self-aligned LDD regions by side etching of the Al-Nd layer in a Al-Nd/Mo terrace-structure gate electrode and using ion implantation at two different energies. However, while the Hatano et al. [24] method is a high-temperature process, requiring the deposition of polysilicon for sidewall formation, the Mishima et al. [25] approach provides poor control of the lateral extension of the LDD regions, relying upon the side etching rate of the Al-Nd layer. To solve these limitations, a process has been proposed by Glasse et al. [9] in which conductive sidewall spacers were formed by n^+ a-Si deposited by plasma enhanced CVD (PECVD), thus reducing the maximum processing temperature compared with the Hatano et al. process. In the followings we show how the introduction of FSA-GOLDD structure can effectively improve both short channel effects and electrical stability.

In Fig. 10 the output characteristics, measured in FSA-GOLDD and SA devices at the gate voltage equal to the threshold voltage (V_g=V_T), are shown. It is evident that the FSA-GOLDD structure effectively mitigates the kink effect, if compared to conventional SA TFTs. This is due to a reduction of the drain electric field and consequent reduction of impact ionization, and best conditions are observed for LDD doses: 6-9 10^{12} cm^{-2}.

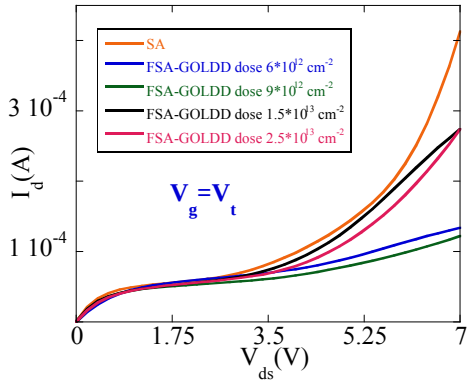

Figure 10. Output characteristics, measured at V_g=V_T in L=1.5 µm SA and FSA-GOLDD TFTs with different LDD (as indicated). Gate oxide thickness was 40 nm for all devices.

To reduce the severe short channel effects present in SA polysilicon TFTs, shown in Figs. 3-5, the conventional approach of reducing the gate oxide thickness was shown to be not effective. In fact, when normalizing the V_T-variations to the oxide thickness there were no major differences, due to enhancement in the floating body effects [26]. To effectively improve the V_T-variations in short channel polysilicon TFTs, the introduction of drain field relief structures could be the only solution. Indeed, Liu at al. [22] reported a substantial reduction in the drain bias induced V_T-variations by introducing LDD regions. Indeed, the FSA-GOLDD structure appears to be quite effective, as evidenced by Fig. 11, showing the ΔV_T dependence upon V_{ds} for SA and FSA-GOLDD architectures, with different LDD doses, having defined $\Delta V_T = V_T(V_{ds}) - V_T(V_{ds}=0.1V)$, with V_T as the gate voltage at which I_d= W/L 3.6 10^{-9} A. The substantial reduction in the V_T-variation at high V_{ds} in FSA-GOLDD TFTs is presumably due to reduced floating body effects.

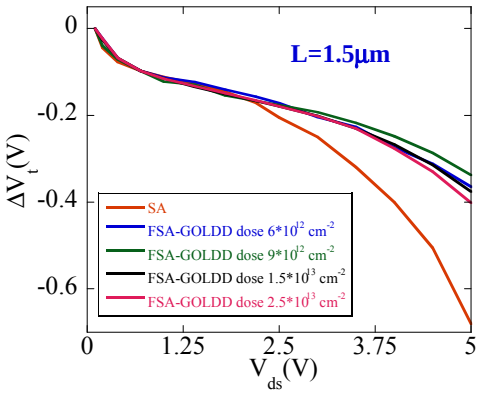

Fig. 11. Threshold voltage variation, ΔV_T, vs V_{ds} for SA and FSA-GOLDD TFTs with different LDD doses (as indicated). Gate oxide thickness was 40 nm for all devices.

To improve hot-carrier induced electrical instability in SA polysilicon TFTs, shown in Figs. 7-9, drain field relief architectures have been proved to be essential [20]. Accelerated stability tests in FSA-GOLDD devices, performed in the hot-carrier regime with similar bias conditions to the SA devices (V_g=V_T and incrementing V_{ds}) are reported in Fig. 12. As can be seen, on current degradation occurs at much higher V_{ds}, if compared to SA TFTs, and the V_{dsc} values for FSA-GOLDD devices are reported in Fig. 9. Electrical stability is considerably improved in FSA-GOLDD devices, if compared to SA TFTs, and appears to be quite sensitive to LDD dose, with optimal LDD doses around 9 10^{12} cm^2.

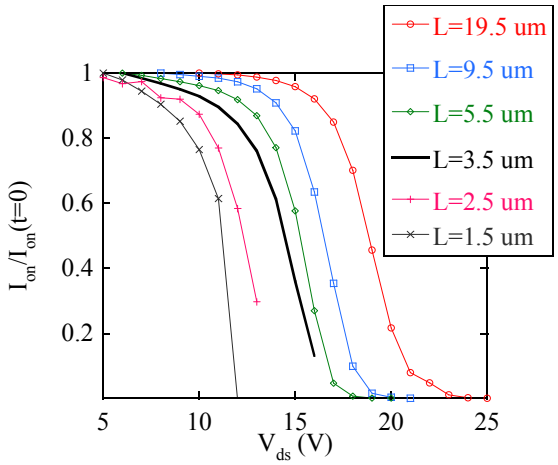

Fig. 12. Relative on-current variation, measured at V_g=5 V and V_{ds}=0.1 V, during accelerated stability tests (see text) performed is FSA-GOLDD polysilicon TFTs with 1.5 10^{13} cm^{-2} LDD dose and different L.

Conclusions

We have shown that channel length reduction, required for improving device performance, can be problematic in conventional SA polysilicon TFTs, due to short channel effects and hot-carrier induced instability. In particular, reducing channel length has a substantial impact on the kink effect, giving output conductance degradation,

shallower subthreshold slope, threshold voltage roll-off and increased dependence upon V_{ds}, and enhanced hot-carrier induced instability. To improve both short channel effects and electrical stability it is essential to introduce drain field relief structures, such as LDD [20, 22] or GOLDD [23]. Indeed, the LDD architecture has been shown to improve short channel effects [22] and hot carrier induced instability [20]. As a drawback, the LDD region increases the parasitic resistance [20], and an attractive alternative is represented by the GOLDD [23] structure, which substantially reduces the parasitic resistance introduced by the LDD regions. However, for the GOLDD structure to be attractive the definition of submicron LDD regions is required. We have analyzed the electrical characteristics of FSA-GOLDD polysilicon TFTs with submicron (0.35 μm) LDD regions and different doping doses. Effective drain field relief was demonstrated by the reduction of short channel effects and the improvement of electrical stability. Best performance in terms of device stability were achieved for LDD doses in the range 9 10^{12} cm^{-2}.

Acknowledgments

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